WHAT IS CLAIMED IS:

1. A data driven type information processing apparatus, comprising:

a self-synchronous transfer control circuit controlling transfer and operating processes of a data packet including at least a destination node number, a generation number, an instruction code and data, by a transfer request signal and a transfer acknowledge signal;

a pipeline register controlled by said self-synchronous transfer control circuit, for storing said data packet;

an input/output control circuit controlling whether said data packet is to be circulated inside or output externally; and

a data packet erasing circuit erasing a data packet stored in at least one of said pipeline registers and outputting other data packets to the outside.

2. The data driven type information processing apparatus according to claim 1, wherein

said data packet erasing circuit includes a master reset input for erasing at least one data packet, adds a new host transfer flag to said data packet, and erases said data packet in accordance with master reset information.

3. The data driven type information processing apparatus according to claim 2, further comprising:

a plurality of host transfer flag operating circuits overwriting a host transfer flag of other data packet in accordance with said master reset information; and

a host transfer flag detecting circuit detecting said host transfer flag.

4. The data driven type information processing apparatus according to claim 2, further comprising:

a host transfer flag operating circuit storing said master reset information, overwriting and outputting a host transfer flag of input other data packet; and

a host transfer flag detecting circuit detecting said host transfer flag.

5. The data driven type information processing apparatus according to claim 2, wherein

said data packet erasing circuit is provided in said input/output control circuit.

6. The data driven type information processing apparatus according to claim 4, wherein

said transfer flag operating circuit is provided in a block nearest to an outlet of the data driven type information processing apparatus, as one of blocks performing said operating process.

7. A data driven type information processing apparatus, comprising:

a self-synchronous transfer control circuit controlling transfer and operating processes of a data packet including at least a destination node number, a generation number, an instruction code and data, by a transfer request signal and a transfer acknowledge signal;

a pipeline register controlled by said self-synchronous transfer control circuit, for storing said data packet;

an input/output control circuit controlling whether said data packet is to be circulated inside or output externally;

a data packet erasing circuit including a master reset input adding a new host transfer flag to the data packet and erasing at least one data packet, for adding a new host transfer flag to said data packet and erasing said data packet in accordance with master reset information;

a plurality of host transfer flag operating circuits overwriting a host transfer flag of other data packet in accordance with said master reset

information; and

a host transfer flag detecting circuit detecting said host transfer flag.

8. A data driven type information processing apparatus, comprising:

a self-synchronous transfer control circuit controlling transfer and operating processes of a data packet including at least a destination node number, a generation number, an instruction code and data, by a transfer request signal and a transfer acknowledge signal;

a pipeline register controlled by said self-synchronous transfer control circuit for storing said data packet;

an input/output control circuit controlling whether said data packet is to be circulated inside or output externally;

a data packet erasing circuit including a master reset input for adding a new host transfer flag to a data packet and erasing at least one data packet, for adding a new host transfer flag to said data packet and erasing said data packet in accordance with master reset information;

a host transfer flag operating circuit storing said master reset information, and overwriting and outputting the host transfer flag of input other data packet; and

a host transfer flag detecting circuit detecting said host transfer flag.